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1. USER GUIDE

a. INTRODUCTION

The Z16 is a low power, very fast access, static memory board capable of supporting 16K of memory on one card.

The card is divided into four blocks of 4K each, which can individually be switch protected, addressed, etc. Each 4K block may be located at any 4K page border, irrespective of the selected address for any other 4K block in the system. (Save only that no two blocks may occupy the SAME address.)

The memory chips employed are the EMM SEMI 4200, which are organized as 4K by 1 bits, and which feature a currently rated access time of 200 nanoseconds. Each 4K block uses 8 memory chips, making a total of 32 for a fully populated board. Due to the treatment of each 4K block as a separate unit, the board may be populated in 4K increments, and thus may serve as an expandable 4,8,12 or 16K memory on the same card.

Physically the board is organized around the "S1ØØ" bus (formerly known as the "ALTAIR™/IMSAI BUS"). It follows the specifications as to the number of TTL loads per line, physical dimensions etc. as have been laid out for this standard. The board operates equally well in either an ALTAIR or an IMSAI, as well as in Technical Design Labs' own line of microprocessors.

Only the finest components and materials have been employed in the manufacture of the Z16, and no surplus components are employed at any location.

The typical power consumption from each of the three voltage supplies for a fully populated 16K board are 200ma from the +5, 120ma from the +12 and 20ma from the -5. Thus, a fully populated 16K board draws little or no more power than "low power" 4K boards available from other manufacturers - thus demonstrating a 4:1 power savings.

b. THEORY OF OPERATION

1. THE 4200 MEMORY CHIP

Exact details of the 4200 memory chip and its specifications etc. are presented in full in the appendix. Those wishing a fuller understanding of this device should refer to those documents which are reproductions of the specifications sheets provided by EMM SEMI.

2. SYSTEM ORGANIZATION

The Z16 card is organized as 4 blocks of 4K each. In essence the card contains 4 separate 4K memory boards. Select, enable logic, power supply etc. are shared.

The four memory blocks are labeled blocks A,B,C and D. U13 to 20 comprise block A; 21 to 28 comprise block B;29 to 36 block C; 37 to 44 block D.

In each block the highest numbered chip (I.E. U20 of block A) of the block contains bit Ø of the word, and the lowest numbered chip contains bit 7 - the remainder stored sequentially between.

3. READING FROM MEMORY

At the beginning of each processor machine cycle, when both Phase 1 and PSYNC are high, these two signals force the output of U3 (74LS20, pin 6) to go low. This signal then triggers the one-shot, U1 (74121, pin 4), which causes $\overline{Q}$ (pin 1) to fall from hi (its normal state) to low and to remain low for a time predetermined by the RC constant of R1 and C3. In this circuit the values of R1 and C3 cause this signal to remain low for 200 nanoseconds.

The $\overline{Q}$ is tied to pins 3,5,9 and 11 of U11 (74LS02) each of which is one of two inputs to a NOR gate. Pins 2,6,8 and 12 of U11 are tied to one of 4 address select jumpers from the address decoding chip U12 (74154). These 4 jumpers are labelled A,B,C and D on both the diagram and the board. These go low when the specific 4K block of memory which they represent is selected. This forces the output of the specific NOR gate (of U11) to go high, while the others remain low.

Each of the four outputs of U11 is then inverted by a section of U10 (7406). Thus three outputs of U10 will be high while the fourth (representing the selected 4K block) will be low.

These outputs are connected to the chip select pins of the 4200s which are arranged in 4K blocks. The 4200 chip select signal is a LOW ($\overline{CS}$), and thus only one of the 4K blocks can be selected at any one time.

The $\overline{Q}$ of the 74121 is also connected to the pin 7s of both U8 and U9 (74173) which is the clock input of these latches. Data may be latched into these chips only when the clocking signal is going from low to hi, which occurs at the end of the 200 nanosecond pulse of the 74121. This delay between the time of selection and the latching in of the data is done to allow the data to stabilize, as is required by the 4200s.

The enabling of the 74173s is controlled by pins 1 and 2 both of which must be LOW for the latched in data to be released. Both pin ones are connected to SMEMR via a gate of U7 (74LS04) which is an inverter. This causes a low to be present on both pin ones when a memory read signal is on the bus.

The signal on pin 2 of both 74173s is controlled by the decoding circuit, U12. When any of the 4 banks is selected the output of U3 (74LS20) goes hi, and the output of this gate is then inverted to a low by a NOR gate configured as an inverter (U2,pins 5 and 6 tied together). Pin 4 of U2 is tied to the pin 2s of both 74173s.

Thus data is being enabled onto the bus from the latches if and only if: a. a memory read signal is on the bus and b. the specific board is selected.

The latching in of the desired data is controlled by the rise of the $\overline{Q}$ of the 74121 from low to hi, which occurs at a time designed to allow the data from the memory chips to have stabilized.

4. WRITING INTO MEMORY

The memory write circuitry functions in much the same manner as the memory read logic. In this case however, no latching of the data occurs.

The chip select circuitry is the same as that which was employed in the memory read logic.

When the memory write line (Bus pin 68 MWRITE) goes high (indicating that a memory write cycle is in progress), this signal is inverted by U2 (74LS02) configured as an inverter. This low signal goes to pin 9 of U2. When the board is selected as previously described, pin 4 of U2 goes low. Pin 4 is connected to pin 8. When both pins 8 and 9 are low, pin 10 goes high. This high signal serves two functions:

a. After being inverted by a gate of U2, it triggers the 74121, setting in motion the same select procedure as described in the memory read section.

b. This hi signal is brought to the pin 12s of the memory chips where it serves the function of a WRITE command. (Pin 12 is R/W, indicating that a HIGH causes a Write.). Thus, this high signal allows the data present on the data out bus to be written into the memory at the address specified on the address bus.

5. MEMORY PROTECT

Switchable memory protect is provided on the board by means of a 4 position mini-dip switch. Each of the 4 switches represents on 4K bank of memory, and the bank names are marked on both the schematic and the board as A,B,C and D.

Opening any of the switches simply disconnects the memory write line (the output of U2, pin 10) from the R/W of the memory chip banks. When held open, the line is held low by resistors 8 thru 11, which allows reading memory to proceed normally.

Provision for additional memory protect facility is made.

CR3 (1N914) is normally connected as shown in the components layout diagram. However, it may alternatively be connected to the hole marked CMW (pin 59 of the bus - CONDITIONAL MEMORY WRITE) when Technical Design Labs' Memory Management Board (an upcoming product) is in use. This board allows software protect capability for your entire system.

6. ADDRESS DECODING

The address decoding function is performed by U12 (74154). This chip takes the four highest address lines and decodes them into one of 16 possibliities. The one possiblity is represented by one of 16 pins going low while the others remain high. Thus each of the

16 pins can represent 1/16th of the total possible memory space in the system, in this case equaling 4K.

Since this memory board is actually the equivalent of 4 separate 4K boards, four jumper plugs are provided which when connected to one of the 16 pins causes the specific 4K block to be selected only when the address which it's pin represents is addressed.

The 16 pins are labelled Ø to F (hexidecimal notation) on the schematic, but are labelled 1 to 16 on the board.

The four 4K banks are labelled A,B,C and D on both the schematic and the board.

Both enable pins (18 and 19) of the 74154 must be low for the board to be enabled. Pin 19 is connected to pin 45 on the bus (SOUT) which goes high only during output operations, thus disabling the board when output operations are in progress. This is not required in an ALTAIR, however, in an IMSAI, a memory write signal is generated during output operations by the front panel, thus making this necessary. The handling of pin 18 is discussed in the section on BANK SWITCHING.

7. BATTERY BACKUP

J1 is provided as a point at which battery power may be applied to the memory. Diodes CR1 and CR2 are provided to prevent backflow of current from the battery onto the bus.

Automatic switching of the battery during line power failure can be achieved by voltage sensing circuitry at the battery. A battery pack with this feature will be made available by Technical Design Labs in the future.

8. BANK SWITCHING

Under control of the upcoming Memory Management board, any 16K board can be made to disappear from the bus. This is achieved by forcing pin 18 of U12 (74154) high, which disables the board. The current version of the board allows two complete 64K banks of memory to coexist in the same mainframe, and be switched under software control using the aforementioned board.

At the bottom of the board directly above the edge fingers and directly beneath the right hand edge of the 74154 are two plated thru holes labelled "X" and "Y". There is a third pad directly between these two.

If the center pad is connected to the "Y" pad, then pin 18 is held low by using part of U7 (74LS04) to invert the output of the 1K pullup resistor. (R12) This is the standard configuration for the board, and is the REQUIRED configuration when the memory management board is NOT in use.

If the center pad is connected to the "X" pad, then pulling down the ABX line ($\overline{ABX}$ = NOT ALTERNATE BANK X Bus pin 60) by the memory management board is necessary for the board to be enabled.

9. THE SCHEMATIC

Several points about the schematic are worthy of mention for the sake of clarity.

a. For the specific pin-outs of the 4200 chips, refer to the spec sheets for these pins located in the appendix.

b. Data Out and Data In are marked on the top row of chips on the schematic. These are the PIN NAMES. They are named in reference to the PROCESSOR. Data Out is DATA OUT FROM THE PROCESSOR. Data In is DATA IN FROM THE PROCESSOR.
   The small arrows under these names are the direction of data flow relative to the memory chips themselves.

c. Rather than draw a confusing jungle of lines, the Address, Data Out and Data In lines are represented by busses. This is possible because these lines are connected in parallel from chip to chip.

c. OPERATION

Operation of the board is very straight forward. Only two advices need be observed:

1. Do not place the address selection jumpers in any address when the bank which the specific jumper represents is unoccupied by chips.

2. When a given bank is unoccupied, the memory protect switch for that bank should be left in the OFF position.

Of course, all the rules which normally govern the general handling of electronic equipment apply - for example, do not insert or remove the board from the motherboard when power is applied, avoid dirt, dust etc. etc.

Operation of the board involves the manipulation of three options. These are:

1. Address selection
2. X or Y bank choice
3. Memory write line choice

The latter two are of consequence only when the Memory Management Board is in use. The normal configurations of these two are:

X or Y bank choice: Center Pad to "Y"
Memory Write Line: CR3 Cathode to RIGHT hole

See the component layout diagram for details of these.

Address selection is set up in the simplest possible fashion. Each of the four banks of 4K (A,B,C and D) is individually addressable at any 4K border in memory. Four plugs (augat pins) attached to wires are soldered into the board above a row of 16 augat pins which lie above U12.

Each of the 16 Augat pins represents one 4K block of memory. The pin on the far right labelled "1" represents the first 4K block of memory (Ø hex; Ø octal). The pin on the far left labelled "16" represents the last 4K block of memory (FØØØ hex; 17ØØØØ octal; 36Ø:ØØØ crazy octal).

Each jumper from one of the 4K blocks may be inserted into any one of the 16 augat pins, at which time that block will be located at whatever 4K border address which the pin you have chosen represents.

Note: Again, remember that if a 4K block of your board is NOT occupied by memory chips, it's jumper plug should not be inserted into one of the 16 augat pins.

In addition to the three options, the protect switch is operated simply. When a switch is ON, the block it represents is UNPROTECTED, and vice-versa.

2. ASSEMBLY

CAUTION

THE Z16 KIT CONTAINS STATIC SENSITIVE DEVICES. THESE ARE ALL OF THE MEMORY CHIPS. DO NOT REMOVE THESE DEVICES FROM THEIR PROTECTIVE TUBES UNTIL NEEDED IN ASSEMBLY. HANDLE ONLY AS PER THE INSTRUCTIONS IN THIS MANUAL. FAILURE TO HEED THIS PRECAUTION MAY RESULT IN PERMENANT DAMAGE TO THESE DEVICES AND AUTOMATICALLY VOIDS THE WARRANTY.

a. GENERAL CONSTRUCTION

It's a good feeling to construct a kit on your own, plug it in, and have it work the first time up. Two factors are of the utmost importance in this: Quality engineering, and careful construction. We've taken care of the engineering, but the construction is up to you. We've listed here some of the construction tips which are considered standard operation in most commercial shops. Following these procedures in your own construction will increase the likelyhood that your kits will work first time, every time.

1. ALWAYS read all of the instructions before starting construction.
2. Always work in a clean, well-lit area.
3. Use only high quality rosin-core solder of a guage similar to the size of the leads being soldered.
4. Ensure that you have all of the parts necessary for a given stage of construction before starting that stage.
5. Use the lowest power soldering iron that will get the job done. A 25 watt iron is quite adequate for most kits using a printed circuit board.
6. Use a fine point soldering iron, and keep the tip clean and well tinned.
7. Avoid overheating the PC board and components.
8. Before soldering, check and make sure that the right component is in the right place. Having to remove and resolder a wrongly placed component is difficult, and there is a great likelyhood that damage to the board or component will occur.

9. Apply the solder to the iron tip, the pad and the component lead at the same time. The solder will melt and flow in a second or two. If it doesn't, stop and find out why before continuing.
10. Use only enough solder to assure electro-mechanical integrity. 1/8th inch or so of the solder supplied with this kit is generally adequate around IC pads and most component leads.
11. Look carefully at each joint both during and after soldering it. If should have a clean, bright appearance. If the surface is rough or dull it might be a cold solder joint. If so, reheat and apply very little or no additional solder.
12. Don't work on construction if you're very tired.
13. Always check the voltages on the appropriate IC pins after soldering and before installing the ICs in their sockets.
14. Never install ICs in sockets when there is voltage on the board.
15. ALWAYS install MOS/CMOS devices LAST, after checking that all else is perfect.
16. NEVER insert the board into it's socket when power is on the machine.

b. HANDLING MOS/CMOS DEVICES

When handled correctly, static damage to these sensitive devices is quite unlikely to occur. The rules for correct handling are simple:

1. Keep everything in contact with everything else. While the ICs are still in the tubes, hold it in your hand, touch both to the table, the PC board, etc. This allows any static to discharge.
2. Work on a conductive surface. Bare grounded metal (a cookie tin or piece of aluminum foil will do.) is best. Glass is very bad, plastics among the worst.
3. Don't wear synthetic clothing. They generate static. Wear Cotton.
4. A high humidity environment is better than a dry one.

These rules are very simple. Remember: the most basic rule is to keep everything in contact with everything else. If you adhere firmly to this one rule and use your common sense, it's very unlikely that you will ever damage a static-sensitive component.

c. PARTS LIST - Z16

U1	- 74121
U2,11	- 74LS02
U3	- 74LS20
U4,5,6,7	- 74LS04
U8,9	- 74173
U10	- 7406
U12	- 74154
U13-44	- 4200
U45	- 7905
U46	- 7812
U47	- 7805
C 1,4	- 47mF, 25V tantalum electrolytic
C 2	- 33mF, 20 V tantalum electrolytic
C 3	- 68pF disc ceramic
C 5	- 220pF disc ceramic
C 6,13	- 3.3 or 4.7mF, 25V tantalum electrolytic
C 7-12	- .1mF disc ceramic, 10V (or same as C 14-26)
C 14-26	- .1mF molded ceramic, 67 volt (black marked 100ns)
R 1	- 3.3K, 1/8th watt (orange, orange,red)
R 2-5,12	- 1K, 1/8th watt (brown, black, red)
R 6	- 220 ohm 1/8th watt (red, red, brown)
R 7-11	- 47K, 1/8th watt (yellow, violet, orange)
J1	- 4 pin molex connector
J2-17	- 16 augat pins
P1-4	- 4 augat pins
CR1,2	- 1N4002
CR3	- 1N914B
S 1-4	- four position mini-dip switch

MISCELLANEOUS

1	- 2 hole heatsink
2	- 5/16" slothead screw, nut, lockwasher
9	- 14 pin low profile sockets
2	- 16 pin low profile sockets
1	- 24 pin low profile socket.
32	- 22 pin low profile sockets (32 sockets are for a 16K board, 24 for 12K etc.)
1	- 6" piece of jumper wire
1	- 6' piece of solder
1	- Z16 PC card

d. DETAILED ASSEMBLY INSTRUCTIONS

( ) 1. Read these instructions through once from beginning to end before continuing.

( ) 2. Inventory all parts against the parts list.

( ) 3. Refer to the board layout diagram and familiarize yourself with the layout.

( ) 4. Examine the PC board carefully for any obvious errors and correct any you may find. (Such as shorted traces etc.). Although numberous quality control checks are done, a slip found now can save many hours of troubleshooting later.

( ) 5. Install the 5 1K resistors (R2-5,12) in their respective locations and solder.

( ) 6. Install the 3.3K resistor (R1) and solder.

( ) 7. Install the five 47K resistors (R7-11) in location and solder.

( ) 8. Install the 220 ohm resistor (R6) and solder.

( ) 9. Install CR1 and CR2 (1N4002) and solder. On CR1 the band goes DOWN. On CR2 the band goes to the LEFT.

( ) 10. Install CR3 (1N914) and solder. If installed in a normal system the band goes to the RIGHT. If installed in a system equipped with Technical Design Labs' Memory Management board, then the band goes to the LEFT and the lead is soldered into the hole labelled CMW.

NOTE: While soldering the diodes, use as little heat as possible. Also, the 1N4002s and 1N914 may be discriminated on the basis of physical size. The 1N4002s are larger.

( ) 11. Install all of the low profile sockets in their locations. Note that ALL 14 and 16 pin sockets are oriented with their pin ones DOWN. The 24 pin socket has the pin one to the RIGHT. ALL 22 pin memory sockets have the pin 1 UP. (IC sockets have a notch or chamfer to indicate pin 1).

( ) 12. Invert the board and solder all of the pins. Make sure that each socket is flush with the board before you solder - otherwise solder may

flow thru the hole when you solder and short out the pins. This is difficult both to trace and to repair.

NOTE: If the sockets tend to fall out when you invert the board, either bend two diagonally opposite pins on each, or preferably, place a piece of thin, stiff cardboard over all of the sockets and turn the board over holding them in place with the cardboard.

( ) 13. Install the 16 augat pins (J2-17) immediatly above the 24 pin socket. The best way to get them in straight is to slip them onto the pins of an old 16 pin dip IC, then bend the row slightly out from the perpendicular, insert all 8 pins into the holes, solder these 8 and then repeat the process for the remaining 8.

( ) 14. Cut 4 pieces of jumper wire, each 1¼ to 1½ inches long. Trim ¼" of insulation off of one end of each, and 3/16ths of insulation off of the other end of each.

( ) 15. Insert the four ends with the 3/16ths" insulation removed into 4 augat pins and solder each. It's best to place the augat pins into empty IC sockets to hold them erect, then place a clean soldering iron tip alongside the pin, then flow the solder onto the wire and the hole at the top of the pin. Use caution not to melt the socket body or to get solder on the tip of the augat pin.

( ) 16. Insert each of the four ¼" trimmed ends into the four holes marked A,B,C and D above the 16 augat pins and solder.

( ) 17. Insert the 68pF capacitor (C3) into it's location alongside U1 and solder. Don't bend this over the socket or you won't be able to get the IC in.

( ) 18. Insert the 220pF capacitor (C5) and solder.

NOTE: The polarity of tantalum electrolytics is usually marked in one of three ways:

a. A + sign next to the voltage rating is usually closest to the + lead.
b. A dot next to a lead indicates that as the + lead.
c. A large dot high on the body of the capacitor- with the dot facing you - the + lead is on the right.

( ) 19. Insert the 33Mf tantalum electrolytic (C2) alongside the heatsink area. Make sure that the polarity is correct. The + lead goes toward the top of the board. Make sure you leave room for the heatsink. Leave the leads a bit long if necessary.

( ) 20. Insert the two 47mF tantalum electrolytics (C1,4) in their respective positions and solder. Make certain that correct polarity is maintained.

( ) 21. Insert the two 3.3 (or 4.7) mF tantalum electrolytics (C6 and 13) in position and solder. The leads may have to be bent out for proper positioning. Insure correct polarity.

( ) 22. Insert the six .1mF 10volt discs (or 6 black molded .1s) (C 7 to 12) in position and solder.

( ) 23. Insert the thirteen .1mF molded 67 volt caps (C 14 to 26) in position and solder.

NOTE: These MUST be the black molded units. Also, if only a 4K board is being constructed, install only C 21 to 26, ommitting C14 to 20.

( ) 24. Install the 7905 voltage regulator (U45). bend the leads 90 degrees, insert in the three holes and solder. Keep the body of the regulator off of the PC board.

( ) 25. Bend the leads of the 7805 and the 7812 voltage regulators (U47 and 46 respectively) down 90 degrees about ¼" from the body.

( ) 26. Insert the screws through the board with the heads on the soldering side of the board, and lay the board down on the table. Place the heatsink over the screws with the longer dimension of hole to edge toward the bottom of the board.

( ) 27. Place the 7805 over the bottom screw with it's pins toward the bottom of the board. Place the lock-washer and the nut over the screw and finger tighten. Have the regulator leads go thru the three holes provided.

( ) 28. Place the 7812 over the top of the two screws with its pins toward the top of the board and repeat the above process.

( ) 29. Tighten both screws. Keep the regulators straight when doing this.

( ) 30. Solder the leads on these two regulators.

NOTE: Heatsink compound may be used on these two regulators if desired, but is generally not necessary due to the low power consumption of the board - and thus cool operation.

( ) 31. Install the 4 pin molex connector to the left of the 7905 and solder. If you're using a high-density motherboard it may be necessary to bend these pins down for adequate board to board clearance.

( ) 32. Install a jumper wire between the center pad and "X" or "Y" depending on which 64K bank the board is to be assigned to. If the Memory Management Board is not in use, solder from center pad to "Y" ONLY.

( ) 33. Trim all leads, including socket pins, down as close to the board as you can using the flat side of diagonal cutters.

( ) 34. Using Tricholrethelyne or some other solvent, plus a stiff ½ inch artist's brush and a clean cloth, clean all residue from the soldering operation off of the board. (When using ANY solvent, NEVER work near an open flame, and ALWAYS work in a WELL ventilated area. The fumes of most solvents are toxic.

NOTE: This is the construction step most often ommitted by the unwise. Cleaning the board throughly will eliminate 95% of those troublesome "solder splashes" that can cause so much trouble, and make the finding of any that remain a "snap".

Start in a corner, applying the solvent liberally by pouring on and "scrubbing" with the brush. BLOT off the remainder with the cloth before the solvent evaporates. (You can't rub over the rough edges.) Repeat if necessary. Continue until the whole board is VERY clean. For final cleaning of the edge fingers, etc. pour some solvent on the rag and wipe clean.

( ) 35. Install the 4 position mini-dip switch in position and solder. It goes with the number one position toward the bottom of the board. (This is done after cleaning because any rosin flux in the switch from the cleaning operation can ruin the switch.

( ) 36. Now examine the board carefully for solder shorts, cold solder joints, unsoldered leads etc. Correct any errors that you find.

( ) 37. Check the board once more to insure that you have all of the components in the correct locations and that they are correctly oriented where applicable.

THIS COMPLETES MECHANICAL ASSEMBLY OF THE BOARD.

You are now ready to continue with the electrical checkout of the board.

( ) 38. Measure the resistances between bus pins 1 and 50, 2 and 50, and 52 and 100. If any of these is Zero, a short circuit is indicated. Locate and correct this.

( ) 39. Insert the board (with no chips other than the regulators installed) in an unoccupied chassis, apply power and measure the voltages at the following locations:

- ( ) a. between the right hand and center pins of the 7805; should measure +5 volts.
- ( ) b. between the left hand and center pins of the 7812; should measure +12 volts.
- ( ) c. between the left hand and right hand pins of the 7905; should measure -5 volts.
- ( ) d. between pins 7 and 14 of U1 to 11, and pins 12 and 24 of U 12 should measure +5 volts.
- ( ) e. between pins 22 and 5 of the 22 pin sockets should measure +12 volts. Between pins 22 and 11 should measure +5 volts. Between pins 22 and 1 should measure -5 volts.

If any of the above voltages differ by more than a very small percent from the above specs, check for shorts, cold solder joints, shorted bypass capacitors, shorted or open pull-up resistors, bad power supply components etc. and correct the problem before continuing.

( ) 40. Insert all of the chips except for the memory chips. Refer to the component layout diagram and insure that the chips are correctly located and properly oriented.

( ) 41. Again plug the board into an unpopulated chassis and turn the power on. Recheck the voltages as per step 39. They should remain the same. A significant change probably indicated a chip which is shorted.

NOTE: At this point you should allow the board to remain on for a few minutes and then check to see if any of the chips (other than the regulators) is getting significantly hotter than those around it. Looking for a "hot" chip is a very useful troubleshooting technique. Many times a malfunctioning board can be repaired easily by using this technique to locate a bad chip.

( ) 42. While following the procedure for the handling of MOS devices, insert one memory chip into the slot for U20, making sure the chip is properly oriented. (Pin one UP). Insert the "A" plug into the augat pin for address zero (pin 1) The other plugs should be out. Place the protect switch for bank "A" in the ON position. The others should be off. Place the memory in the chassis along with the processor and no other boards.

NOTE: You are starting by checking only one memory chip because these chips are EXPENSIVE. In small quantities they cost nearly as much as an 8080 processor!

( ) 43. Apply power, reset, and examine memory location zero. Now try alternatly depositing ones and zeros into the memory for bit ZERO. You should be able to cause this light to go on and off.

NOTE: If your system has no front panel you'll have to do this under monitor program control.

( ) 44. If you cannot deposit this bit, recheck the board for any of the possible errors, such as misaligned chips, chips in wrong locations, diodes placed backwards etc etc. If still no luck you probably have an undetected solder short, faulty component or some such.

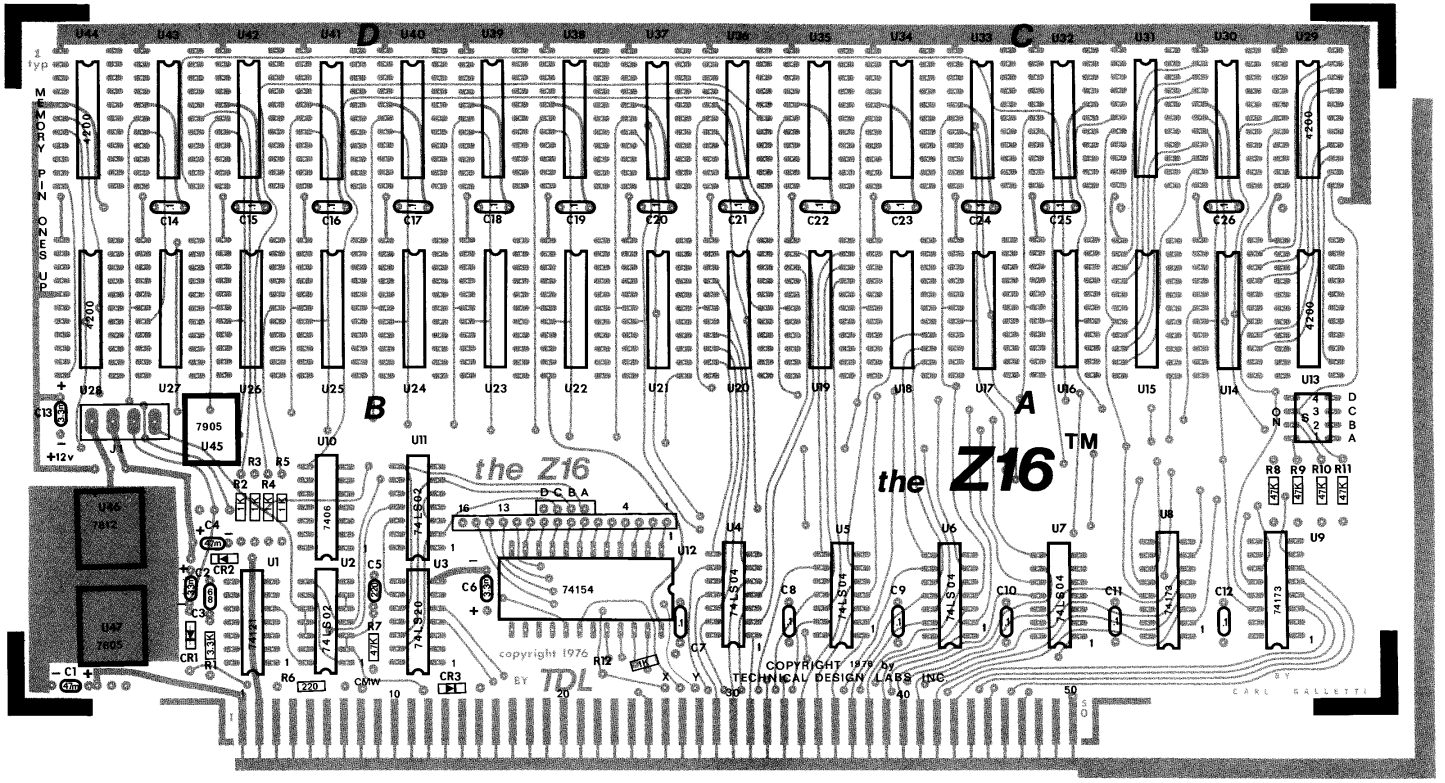
( ) 45. Once you are successful with step 43, insert the remainder of the memory chips into bank A.

( ) 46. Now try to deposit and deposit next starting with all zeros, then bit one by itself, then bit 2,3 and so on up to bit seven. This determines if the data in and out lines are correctly functioning. A problem here usually indicates that one or more of these lines are shorted, or that the associated chips are either wrongly inserted or bad.

( ) 47. Next try to examine from zero on up - using the examine next switch. This tests that the address lines are in order. A problem here indicates problems similar to the above.

( ) 48. If the above checks out, then proceed to insert the chips in the remainder of the banks which you intend to populate.

This completes construction and mechanical as well a logical operation checkout of the board.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TECHNICAL DESIGN LABS INC
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MEMORY PIN ONE'S UP
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74154
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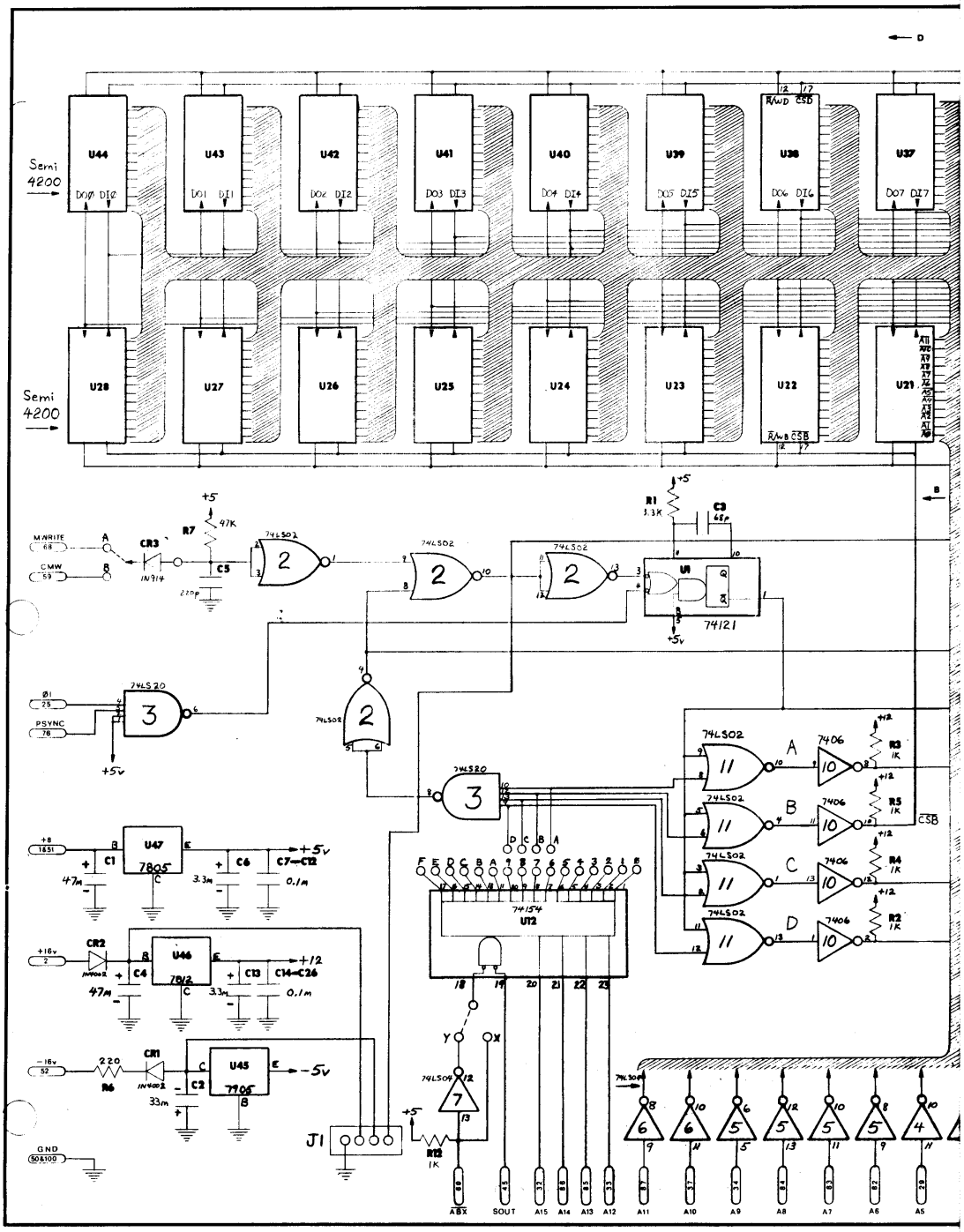
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U44
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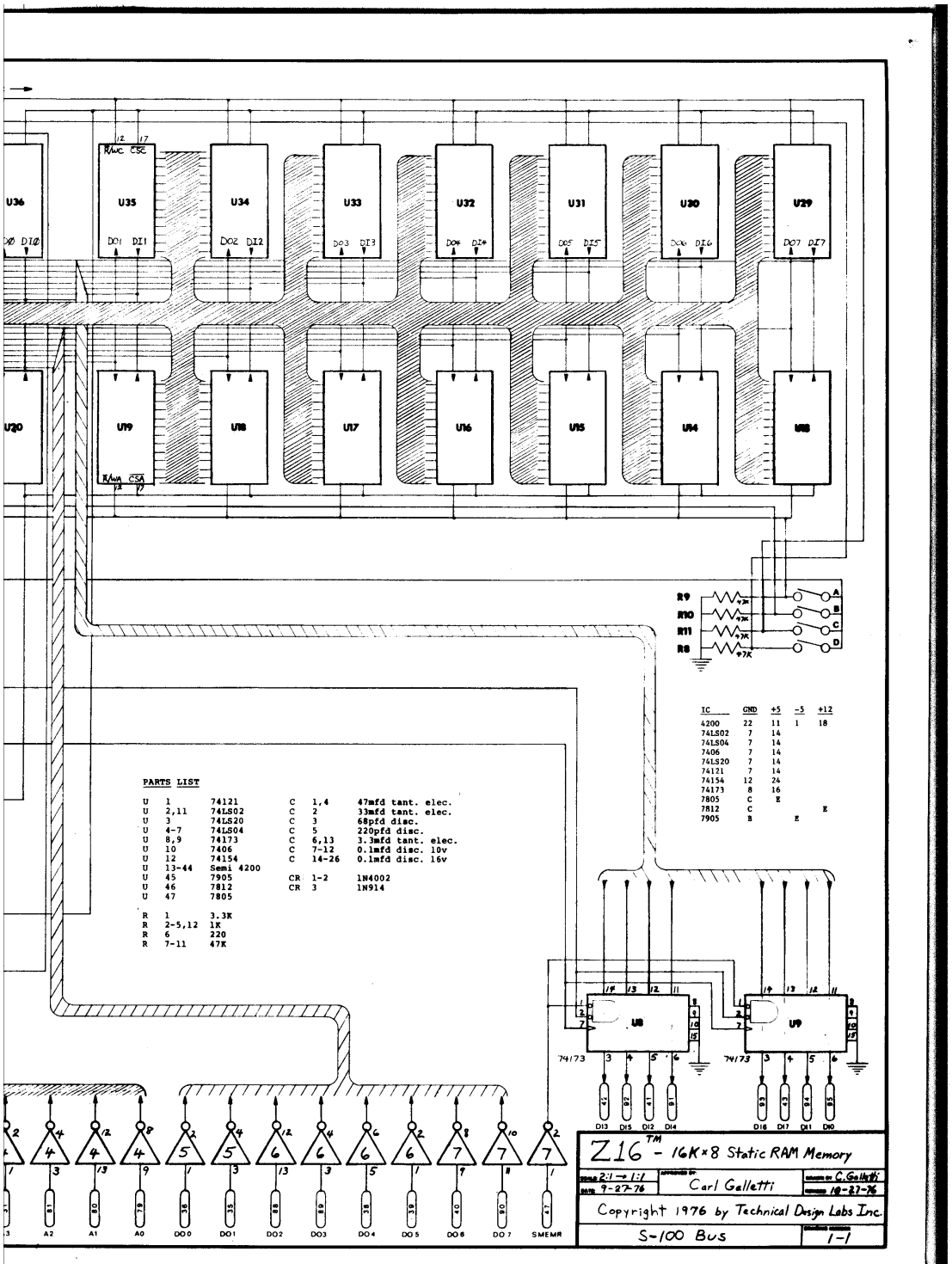
U22
U21
74LS02
74LS20
74121
74154
7406
7805
7905
7815
7915
U1
U12
U45
U46
U47
R1 3.3K
C3 68p
R7 47K
CR3 IN914
C5 220p
R6 220
CR1 IN4002
CR2 IN4002
C1 47m
C2 33m
C4 47m
C6 3.3m
C13 3.3m
C7-C12 0.1m
C14-C26 0.1m
R12 1K
R2 1K
R3 1K
R4 1K
R5 1K
MWRITE
CMW
Ø1
PSVNC
GND
+5v
+12
-16v
-5v
J1
A
B
C
D
CSB
ABX
SOUT
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5



PARTS LIST

U	1	74121	C	1,4	47mfd tant. elec.
U	2,11	74LS02	C	2	33mfd tant. elec.
U	3	74LS20	C	3	68pfd disc.
U	4-7	74LS04	C	5	220pfd disc.
U	8,9	74173	C	6,13	3.3mfd tant. elec.
U	10	7406	C	7-12	0.1mfd disc. 10v
U	12	74154	C	14-26	0.1mfd disc. 16v
U	13-44	Semi 4200			
U	45	7905	CR	1-2	1N4002
U	46	7812	CR	3	1N914
U	47	7805			
R	1	3.3K			
R	2-5,12	1K			
R	6	220			
R	7-11	47K			

IC	GND	+5	-5	+12
4200	22	11	1	18
74LS02	7	14		
74LS04	7	14		
7406	7	14		
74LS20	7	14		
74121	7	14		
74154	12	24		
74173	8	16		
7805	C		E	
7812	C			E
7905	B		E	

Z16™ - 16K×8 Static RAM Memory

SCALE 2:1 → 1:1	APPROVED BY Carl Galletti	DRAWN BY C. Galletti
DATE 9-27-76		REVISED 10-27-76

S-100 Bus

1-1

g. MEMORY CHECKOUT

Now that your board is finished it is wise to verify not only that the board is operating normally, but that the memory chips themselves are accurately writing and reading the memory you actually desire. In manufacturing, finding one chip out of a 100 lot being bad is not uncommon. The following is designed to help you verify the accuracy of your memory. Any bad chips returned to Technical Design Labs will be replaced immediatly as per the terms of the warranty.

For those of you whose system is equipped with the ZPU, use of either the ZAP (1K) or ZAPPLE (2K) monitors is by far the easiest means of running a memory check.

With the ZAP monitor, use of the J command is your easiest means of locating hard memory failures. Simply type the J command followed by the memory block to be tested and hit return. If all is OK, the monitor will perform a line feed and print a period (.).

If one or more bits are bad, the response will be the Address of the bad bit, followed by the bit pattern recorded at that address.

For example, if the monitor responds with:

ØF77 00100000

this means that the third bit at location ØF77 is bad.

Address ØF77 is in block A (when it's addressed at zero). And the third bit is contained in U18. Therefore you may conclude that U18 is at fault. Replace this one with a chip from a higher bank and return it for replacement.

While this test is excellent for the location of "hard" memory failures, it is not a dynamic test, so it is not 100% definitive. User's of the ZAPPLE monitor have an additional tool at hand which does provide a dynamic test.

With the monitor in use, MOVE the monitor from it's working address to an address contained within the memory being tested. Now use the VERIFY command to verify that the data remained the same. Positive results on this test are a very strong indication that all is well.

There follows the source code for a memory test program designed to allow a thorough verification of the validity of your memory. This is provided for those who do not have either the ZAP or ZAPPLE monitors available, or as a supplement to these facilities.

A paper tape in absolute hex format is provided with this kit.

```
                        .TITLE  *8080/Z-80 MEMORY TEST VERSION 1.0*
                        ;
                        ;       TECHNICAL DESIGN LABS, INC.
                        ;       RESEARCH PARK
                        ;       PRINCETON, NJ. 08540
                        ;
                        ;       SEPTEMBER 1976 -R.A.  609
                        ;
                        ; THERE IS NO MEMORY TEST AVAILABLE THAT CAN BE
                        ; CALLED THE "DEFINITIVE MEMORY TEST PROGRAM".
                        ;
                        ; THE FOLLOWING IS ONE THAT WILL AT LEAST PROVIDE
                        ; SOME DIAGNOSTIC ASSISTANCE, AS WELL AS SOME
                        ; DEGREE OF CONFIDENCE.
                        ;
                        ; THE BEST TEST IS A FEW WEEKS OF TIME, RUNNING
                        ; THE SYSTEM, AND EXERCISING THE SYSTEM AS A
                        ; WHOLE.  YOU WILL KNOW SOON ENOUGH IF THE
                        ; MEMORY IS SOUND.
                        ;
                        ; THIS PROGRAM STARTS AT ADDRESS 0100H. (YOU MAY TEST
                        ; MEMORY FROM 0400H ON UPWARDS. MAX=0FFFFH). THE
                        ; TAPE IS SENT IN THE INTEL STYLE HEX FILE FORMAT,
                        ; AND CAN BE READ BY EITHER THE APPLE/ZAPPLE MONITORS,
                        ; (OR ZAP), OR BY USING THE BOOT LOADER PROVIDED.
                        ; THE PROGRAM IS SELF-CONTAINED. IT CAN BE EASILY
                        ; PATCHED FOR ANOTHER I/O SYSTEM IF NEED BE.  IT IS
                        ; CONFIGURED FOR THE STANDARD PORT ZERO ALTAIR-STYLE
                        ; TELETYPE I/O.
                        ;
                        ; THE PROGRAM WILL SIGN ON, AND ASK FOR THE RANGE.
                        ; THIS SHOULD BE GIVEN IN HEX.  "START"[,]"FINISH".
                        ; IT WILL TEST CONTINOUSLY UNTIL A CONTROL-C IS
                        ; SEEN ON THE KEYBOARD.  ERRORS WILL BE PRINTED OUT
                        ; WITH THE ADDRESS OF THE ERROR, THE TEST BYTE,
                        ; AND THE MEMORY ERROR PATTERN. THE BITS THAT
                        ; DON'T AGREE ARE "1".  ALSO, WHILE THE TEST IS IN
                        ; PROGRESS, A NUMBER WILL BE PRINTED ON THE
                        ; CONSOLE FOR EACH LOOP THROUGH ALL 13 TESTS.
                        ;
                        ;       <CONSTANTS>
                        ;
0000                    STAT=   0H      ;STATUS PORT
0001                    DATA=   1H      ;DATA PORT
0080                    TTBE=   80H     ;XMIT EMPTY
0001                    TTDA=   1       ;RECIEVE DATA AVAILABLE
000D                    CR=     0DH
000A                    LF=     0AH
                        ;
                        ;       <PROGRAM BEGINS HERE>
                        ;
0100                    .LOC    0100H           ;LOCATE AT PAGE ONE
                        .PABS                   ;ABSOLUTE OBJECT FILE
                        ;
0100  31 0344           START:  LXI     SP,STACK        ;SET UP A STACK
```

```
0103  21 02EC          LXI     H,MSG0  ;SIGN ON MESSAGE
0106  CD 02DF          CALL    TYPE
0109  21 032E          LXI     H,TEMP  ;INITIALIZE TEMP. VALUES
010C  3600            MVI     M,0
010E  23              INX     H
010F  3640            MVI     M,40H
0111  0602            MVI     B,2     ;GET TWO ADDRESSES
0113  21 0000  EXPR:  LXI     H,0
0116  CD 02D1  EX0:   CALL    KBD     ;GET PARAMETERS
0119  4F              MOV     C,A
011A  CD 0129  EX1:   CALL    NIBBLE  ;CONVERT TO HEXADECIMAL
011D  DA 0139         JC      EX2
0120  29              DAD     H       ;CONVERT TO BINARY
0121  29              DAD     H
0122  29              DAD     H
0123  29              DAD     H
0124  B5              ORA     L
0125  6F              MOV     L,A
0126  C3 0116         JMP     EX0
0129  D630    NIBBLE: SUI     '0'     ;ASCII TO HEX
012B  D8              RC
012C  FE17            CPI     'G'-'0'
012E  3F              CMC
012F  D8              RC
0130  FE0A            CPI     10
0132  3F              CMC
0133  D0              RNC
0134  D607            SUI     'A'-'9'-1
0136  FE0A            CPI     10
0138  C9              RET
0139  79        EX2:  MOV     A,C
013A  CD 02BE         CALL    CHK
013D  EB              XCHG
013E  05              DCR     B       ;TWO ADDRESSES YET?
013F  C2 0113         JNZ     EXPR
0142  3E4F            MVI     A,'O'   ;ALL OK
0144  CD 029E         CALL    SEND
0147  3E4B            MVI     A,'K'
0149  CD 029E         CALL    SEND
014C  CD 02B4         CALL    CRLF
                ;
014F  E5        DOIT: PUSH    H       ;START TESTING
0150  36AA      ..1:  MVI     M,0AAH  ;10101010 PATTERN
0152  23              INX     H
0153  3655            MVI     M,55H   ;01010101 PATTERN
0155  CD 0249         CALL    HILO    ;RANGE SATISFIED YET?
0158  D2 0150         JNC     ..1
015B  CD 023C         CALL    DELAY   ;BITS ARE TRICKY AT TIMES
015E  E1              POP     H       ;RESTORE START POINTER
015F  E5              PUSH    H       ;SAVE IN STACK
0160  3EAA      ..2:  MVI     A,0AAH
0162  46              MOV     B,M     ;PICK UP MEMORY BYTE
0163  B8              CMP     B       ;NOW VERIFY MEMORY
0164  C4 024F         CNZ     ERROR   ;TELL IF BAD
0167  23              INX     H
```

```
0168  3E55            MVI     A,55H
016A  46              MOV     B,M
016B  B8              CMP     B
016C  C4 024F         CNZ     ERROR
016F  CD 0249         CALL    HILO    ;RANGE TEST
0172  D2 0160         JNC     ..2
0175  E1              POP     H
0176  E5              PUSH    H
0177  3655      ..3:  MVI     M,055H  ;REVERSE (CHECKERBOARD)
0179  23              INX     H
017A  36AA            MVI     M,0AAH
017C  CD 0249         CALL    HILO
017F  D2 0177         JNC     ..3
0182  CD 023C         CALL    DELAY
0185  E1              POP     H
0186  E5              PUSH    H
0187  3E55      ..4:  MVI     A,55H
0189  46              MOV     B,M
018A  B8              CMP     B
018B  C4 024F         CNZ     ERROR
018E  23              INX     H
018F  3EAA            MVI     A,0AAH
0191  46              MOV     B,M
0192  B8              CMP     B
0193  C4 024F         CNZ     ERROR
0196  CD 0249         CALL    HILO
0199  D2 0187         JNC     ..4
019C  E1              POP     H
019D  E5              PUSH    H
019E  36FF      ..5:  MVI     M,0FFH  ;ALL ONES
01A0  CD 0249         CALL    HILO
01A3  D2 019E         JNC     ..5
01A6  CD 023C         CALL    DELAY
01A9  E1              POP     H
01AA  E5              PUSH    H
01AB  3EFF      ..6:  MVI     A,0FFH
01AD  46              MOV     B,M
01AE  B8              CMP     B
01AF  C4 024F         CNZ     ERROR
01B2  CD 0249         CALL    HILO
01B5  D2 01AB         JNC     ..6
01B8  E1              POP     H
01B9  E5              PUSH    H
01BA  0E00            MVI     C,0     ;SEQUENTIAL NUMBERS TEST
01BC  71        ..7:  MOV     M,C     ;START WITH ZERO
01BD  0C              INR     C
01BE  CD 0249         CALL    HILO
01C1  D2 01BC         JNC     ..7
01C4  CD 023C         CALL    DELAY
01C7  E1              POP     H
01C8  E5              PUSH    H
01C9  0E00            MVI     C,0
01CB  79        ..8:  MOV     A,C
01CC  0C              INR     C
01CD  46              MOV     B,M
```

```
01CE  B8              CMP     B
01CF  C4 024F         CNZ     ERROR
01D2  CD 0249         CALL    HILO
01D5  D2 01CB         JNC     ..8
01D8  E1              POP     H
01D9  E5              PUSH    H
01DA  74        ..9:  MOV     M,H     ;PAGE DECODING TEST
01DB  24              INR     H
01DC  CD 024A         CALL    HILO+1  ;JUST INCREMENT H REG
01DF  D2 01DA         JNC     ..9
01E2  CD 023C         CALL    DELAY
01E5  E1              POP     H
01E6  E5              PUSH    H
01E7  7C        ..A:  MOV     A,H
01E8  46              MOV     B,M
01E9  B8              CMP     B
01EA  C4 024F         CNZ     ERROR
01ED  24              INR     H
01EE  CD 024A         CALL    HILO+1
01F1  D2 01E7         JNC     ..A
01F4  E1              POP     H
01F5  E5              PUSH    H
01F6  7E        ..B:  MOV     A,M     ;FAST COMPLIMENT & TEST
01F7  2F              CMA
01F8  77              MOV     M,A
01F9  46              MOV     B,M
01FA  B8              CMP     B
01FB  C4 024F         CNZ     ERROR
01FE  3600            MVI     M,00    ;ZERO MEMORY TEST
0200  CD 0249         CALL    HILO
0203  D2 01F6         JNC     ..B
0206  CD 023C         CALL    DELAY
0209  E1              POP     H
020A  E5              PUSH    H
020B  AF        ..C:  XRA     A       ;TEST FOR STILL ZERO
020C  46              MOV     B,M
020D  B8              CMP     B
020E  C4 024F         CNZ     ERROR
0211  CD 0249         CALL    HILO
0214  D2 020B         JNC     ..C
0217  CD 022D         CALL    STOP    ;SEE IF CONSOLE WANT TO ABORT
021A  21 032F         LXI     H,TEMPO ;PICK UP COUNTER
021D  7E              MOV     A,M
021E  E607            ANI     7
0220  F630            ORI     '0'     ;COUNT OF THE NUMBER OF
0222  CD 029E         CALL    SEND    ;# TIMES THROUGH THE MEMORY
0225  34              INR     M
0226  FC 02B2         CM      LINE    ;CRLF EACH 64 CHARACTER
0229  E1              POP     H
022A  C3 014F         JMP     DOIT    ;DO ALL OF THIS AGAIN
                ;
                ;       <SUBROUTINES>
                ;
022D  DB00      STOP: IN      STAT    ;SEE IF CONSOLE WANTS TO STOP
022F  E601            ANI     TIDA
```

```
0231  C0              RNZ
0232  DB01            IN      DATA
0234  E67F            ANI     7FH
0236  FE03            CPI     3       ;CONTROL-C
0238  C0              RNZ
0239  C3 0100         JMP     STARI   ;INSERT A MONITOR JUMP HERE
023C  26FF    DELAY:  MVI     H,0FFH  ;CAN BE SHORTENED IF TESTING
023E  2EFF    DEL0:   MVI     L,0FFH  ;LARGE AMOUNTS OF MEMORY
0240  2D              DCR     L
0241  C2 0240         JNZ     .-1
0244  25              DCR     H
0245  C2 023E         JNZ     DEL0
0248  C9              RET
0249  23      HILO:   INX     H
024A  7B              MOV     A,E
024B  95              SUB     L
024C  7A              MOV     A,D
024D  9C              SBB     H
024E  C9              RET
                ;
024F  F5      ERROR:  PUSH    PSW     ;SAVE TEST BYTE
0250  3A 032E         LDA     TEMP    ;SEND MESSAGE?
0253  B7              ORA     A
0254  C2 0263         JNZ     ..NO    ;NO
0257  2F              CMA
0258  32 032E         STA     TEMP    ;MESSAGE SENT
025B  E5              PUSH    H
025C  21 030C         LXI     H,MSG
025F  CD 02DF         CALL    TYPE
0262  E1              POP     H
0263  7C      ..NO:   MOV     A,H     ;SEND HIGH BYTE OF ADDRESS
0264  CD 028D         CALL    WRIT2
0267  7D              MOV     A,L     ;AND LOW BYTE
0268  CD 028D         CALL    WRIT2
026B  CD 02AA         CALL    BLK     ;SPACE OVER
026E  F1              POP     PSW     ;GET TEST BYTE
026F  F5              PUSH    PSW     ;SAVE AGAIN
0270  CD 028D         CALL    WRIT2   ;PRINT IT
0273  CD 02AA         CALL    BLK
0276  F1              POP     PSW     ;GET BYTE BACK
0277  A8              XRA     B       ;GET BAD BIT LOC.
0278  0608            MVI     B,8     ;NUMBER OF BITS/BYTE
027A  17      ..BIT:  RAL             ;SET/RESET CARRY
027B  F5              PUSH    PSW     ;SAVE THE BAD BITS
027C  3E18            MVI     A,('0')/2
027E  8F              ADC     A       ;MAKE '0' OR '1'
027F  CD 029E         CALL    SEND
0282  F1              POP     PSW     ;GET BAD BYTE
0283  05              DCR     B
0284  C2 027A         JNZ     ..BIT   ;PUMP 'EM OUT.
0287  CD 02B4         CALL    CRLF
028A  C3 022D         JMP     STOP    ;SEE IF CONSOLE WANTS TO STOP
028D  F5      WRIT2:  PUSH    PSW     ;BINARY TO ASCII HEX
028E  0F              RRC
028F  0F              RRC
```

```
0290  0F              RRC
0291  0F              RRC
0292  CD 0296         CALL    ..1ST
0295  F1              POP     PSW
0296  E60F    ..1ST:  ANI     0FH     ;THIS DAA IS CUTE
0298  C690            ADI     90H
029A  27              DAA             ;(THANKS, INTEL)
029B  CE40            ACI     40H
029D  27              DAA
                ;
029E  F5        SEND:   PUSH    PSW     ;MAIN TELETYPE OUTPUT
029F  DB00      ..S:    IN      STAT
02A1  E680              ANI     TTBE
02A3  C2 029F           JNZ     ..S
02A6  F1                POP     PSW
02A7  D301              OUT     DATA
02A9  C9                RET
02AA  3E20      BLK:    MVI     A,' '
02AC  CD 029E           CALL    SEND
02AF  C3 029E           JMP     SEND
02B2  3640      LINE:   MVI     M,40H   ;RESET TEST COUNTER
02B4  3E0D      CRLF:   MVI     A,CR    ;CRLF ON CONSOLE
02B6  CD 029E           CALL    SEND
02B9  3E0A              MVI     A,LF
02BB  C3 029E           JMP     SEND
                ;
02BE  FE2C      CHK:    CPI     ','     ;SPACE OR COMMA BETWEEN ADDR
02C0  C8                RZ
02C1  FE20              CPI     ' '
02C3  C8                RZ
02C4  FE0D              CPI     CR      ;TERMINATION?
02C6  C2 0100           JNZ     START   ;HHMMM....
02C9  78                MOV     A,B
02CA  3D                DCR     A
02CB  C2 0100           JNZ     START   ;TOO MANY OR TOO FEW PARAMS
02CE  C3 02B4           JMP     CRLF
                ;
02D1  DB00      KBD:    IN      STAT    ;MAIN TELETYPE INPUT ROUTINE
02D3  E601              ANI     TTDA
02D5  C2 02D1           JNZ     KBD
02D8  DB01              IN      DATA
02DA  E67F              ANI     7FH     ;CLR PARITY
02DC  C3 029E           JMP     SEND    ;ECHO INPUT
                ;
02DF  CD 022D   TYPE:   CALL    STOP    ;TEST FOR AN ABORT
02E2  7E                MOV     A,M     ;MESSAGE SENDER ROUTINE
02E3  B7                ORA     A
02E4  C8                RZ
02E5  CD 029E           CALL    SEND
02E8  23                INX     H
02E9  C3 02DF           JMP     TYPE
                ;
                ;       <MESSAGES>
                ;
02EC  0D0A      MSG0:   .BYTE   CR,LF
```

```
02EE  4D454D4F52          .ASCII  'MEMORY TEST VER. 1.0'
0302  0D0A                .BYTE   CR,LF
0304  52414E4745          .ASCII  'RANGE- '
030B  00                  .BYTE   00
030C  0D0A        MSG:    .BYTE   CR,LF
030E  4144445220          .ASCII  'ADDR TEST 76543210  -BAD BITS'
032B  0D0A00              .BYTE   CR,LF,00
                  ;
032E  00          TEMP:   .BYTE   0
032F  40          TEMP0:  .BYTE   40H       ;COUNTER
0344              STACK=  .+20
                  ;
                  .END
```

+++++ SYMBOL TABLE +++++

BLK	02AA	CHK	02BE	CR	000D	CRLF	02B4
DATA	0001	DEL0	023E	DELAY	023C	DOIT	014F
ERROR	024F	EX0	0116	EX1	011A	EX2	0139
EXPR	0113	HILO	0249	KBD	02D1	LF	000A
LINE	02B2	MSG	030C	MSG0	02EC	NIBBLE	0129
SEND	029E	STACK	0344	START	0100	STAT	0000
STOP	022D	TEMP	032E	TEMP0	032F	TTBE	0080
TTDA	0001	TYPE	02DF	WRIT2	028D		

3. GENERAL INFORMATION

a. CUSTOMER SERVICE

Customer service falls into two broad categories:

1. Equipment troubleshooting
2. User applications counseling

In the case of equipment troubleshooting when you wish to return the unit for factory service, the following procedure should be adhered to whether the unit is under warranty or not.

1. Write up the exact symptoms of the problem. Give exact details of what you observed, what you noticed, what you were doing when the problem was first noticed, etc.
2. Describe the system you had in operation when the problem developed. Note the kind of mainframe, accessory boards in use, program being run, switch positions, peripheral connections etc. Also note if the other boards appear to be functioning normally.
3. Describe what you have done to try and handle the problem, Please be as specific as possible.
4. Pack the unit well (you would be wise to keep the shipping carton and materials this unit came in for this possibility.) and return it postpaid to Technical Design Labs.
5. If the unit is NOT under warranty, enclose an authorization to repair and bill to whatever dollar limit beyond which you would want to be informed before we continue.
6. If the unit is under warranty, it will be treated as per the conditions as laid out in the warranty.

In the case of user applications counseling, the service is generally free of charge. This service is designed to aid you in applications where your own ability or experience is not sufficient to provide the answer. This is not intended to provide a borad educational service of a general nature. Rather it is designed to answer specific applications problems where a "how to: may not be clear

to a less than very experienced computerist. If your questions are specific, you will receive an answer as quickly as possible.

For questions of a more general nature, such as those that might repeat from many users, or for items which we feel would be of interest to a broader public, such will be printed up and distributed as part of the Z-80 users' group Newsletter which has been established. The newsletter will publish any information on program development, novel computer applications, hardware configurations etc. which fall into the above broad interest category. We hereby solicit any such submissions as you may wish to provide.

It is not currently possible to offer aid other than of a general nature in the debugging of user prepared software. We will however be glad to offer advice when feasible.

A software library is currently being established for your use, and if you have any software whcih you feel would benefit others, please feel free to submit this for our inclusion.

Listings of available software will be published in the Users Group Newsletter.

b. WARRANTY

TECHNICAL DESIGN LABS INC., in recognition of its responsibility to provide quality components and adequate instructions for their proper use and assembly, warrants it's products as follows:

All components sold by Technical Design Labs Inc., (hereinafter referred to as TDL) are first quality prime and are procured from reputable distributors and/or factories and their representatives, and any part which fails because of defects in manufacture or material will be replaced at no charge for a period of 3 months for kits, and one year for assembled products following the date of purchase measured from the date of receipt. For replacement, the defective part must be returned to TDL postpaid within the warranty period.

Any malfunctioning unit or subunit, purchased as a kit and returned to TDL within the 3 month warranty period, which in the judgement of TDL has been constructed with care, and has not been subject to electrical or mechanical abuse, will be restored to proper operating condition or replaced at TDL's discretion and returned, with a minimal charge to cover postage.

Any units or subunits purchased as a kit and returned to TDL within the 3 month warranty period, which in the opinion of TDL is not covered by the above conditions will be repaired and returned at a cost commensurate with the work required. In no case will this charge exceed $30.00 without prior notification and approval of the owner.

Any unit or subunit, purchased as assembled units are guaranteed to meet the specifications in effect at the time of manufacture for a period of at least one year following purchase. These units are additionally guaranteed against defects in materials or workmanship for the same one year period. All warranted factory assembled units returned to TDL postpaid will be repaired and returned without charge providing only that no evidence of electrical or mechanical abuse exists.

This warranty is made in lieu of all other warranties expressed or implied and is limited in any case to the repair or replacement of the unit or subunit involved.

TIMING DIAGRAMS

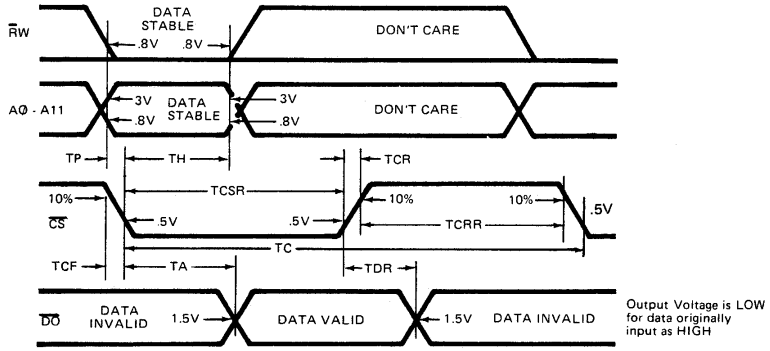


Figure 1 – Read Cycle

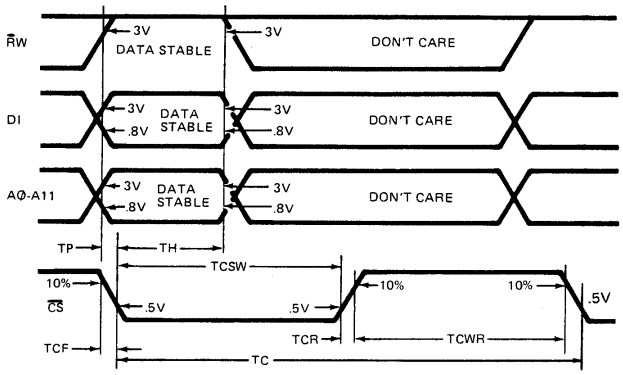
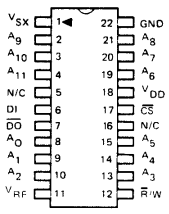


Figure 2 – Write Cycle

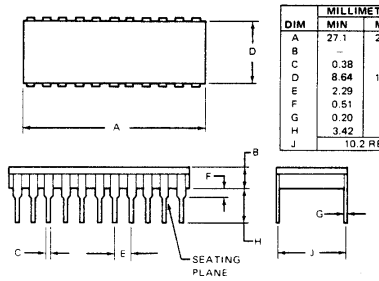
22 PIN DUAL IN-LINE

PIN	SYMBOL	FUNCTION
1	V_{SX}	Supply Voltage (–5V)
2	A_9	Address Input
3	A_{10}	Address Input
4	A_{11}	Address Input
5	N/C	
6	D_I	Data In
7	$\overline{D_O}$	Data Out
8	A_0	Address Input
9	A_1	Address Input
10	A_2	Address Input
11	V_{RF}	Supply Voltage (5V)
12	$\overline{R}/W$	Read/Write Input
13	A_3	Address Input
14	A_4	Address Input
15	A_5	Address Input
16	N/C	
17	$\overline{CS}$	Chip Select
18	V_{DD}	Supply Voltage (12V)
19	A_6	Address Input
20	A_7	Address Input
21	A_8	Address Input
22	GND	Ground

TOP VIEW



PIN ASSIGNMENT



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	27.1	27.8	1.065	1.095
B	–	3.56	–	0.140
C	0.38	0.53	0.015	0.021
D	8.64	10.8	0.340	0.425
E	2.29	2.79	0.090	0.110
F	0.51	1.27	0.020	0.050
G	0.20	0.30	0.008	0.012
H	3.42	3.93	0.135	0.155
J	10.2 REF		0.4 REF	

CERAMIC PACKAGE DIMENSIONS

ABSOLUTE MAXIMUM RATINGS (See Note 1) (Referenced to GND)

Rating	Symbol	Value	Unit
Supply Voltages	V_{DD}	−.5 to +15	Vdc
	V_{RF}	−.5 to +7	Vdc
	V_{SX}	+.5 to −7	Vdc
Input & Output Voltages (Except Chip Select)	V_I, V_O	V_{SX} to +15	Vdc
Chip Select Input Voltage	V_{CS}	V_{SX} to +15	Vdc
Power Dissipation	P_D	1.6 (Note 2)	W
Operating Ambient Temperature Range	T_{AMB}	0 to +70	°C
Storage Temperature Range	–	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended or maximum voltages for extended periods of time could affect device reliability.

NOTE 2: At 25°C ambient. Derate 13.5m w/°C.

RECOMMENDED OPERATING CONDITIONS T_{AMB} = 0°C to 70°C

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{DD}	11.4	12.0	12.6	Vdc
Output Reference Voltage	V_{RF}	4.75	5.0	5.25	Vdc
Substrate Voltage	V_{SX}	−4.5	−5	−5.5	Vdc
Input High Level	V_{IH}	3	–	5.25	Vdc
Input Low Level	V_{IL}	0	–	0.8	Vdc
Chip Select High Level	V_{CH}	V_{DD} −3	V_{DD}	V_{DD}+3	Vdc
Chip Select Low Level	V_{CL}	0	–	0.5	Vdc

DC ELECTRICAL CHARACTERISTICS (Full Operating voltage & temperature range unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Input Current	I_{IN}	0	±10	±100	μA	V_{IN} = 0.5V or 5.0V
Chip Select Input Current	I_{CS}	–	±10	±100	μA	V_{CS} = 0.5V or 12V
Output "Low" Voltage	V_{OL}	–	0.3	0.5	Vdc	I_O = 2.0mA Fig. 5
Output "High" Voltage	V_{OH}	2.7	3.5	V_{RF}	Vdc	I_O = 500μA Fig. 5
Output Current (Unselected)	I_{DO}	–	–	−50	μA	V_{OL} = 2.7V, V_{CS} = +12V
Supply Current (Selected and Averaged over one cycle) CSW = 215 nsec TC = 400 nsec For Other Conditions, See Figure 3	I_{DD}	–	36	50	mA	V_{DD} = +12V V_{RF} = +5V V_{SX} = −5V T_{AMB} = 25°C
Supply Current (Unselected) T_{AMB} = 25°C	I_{DDU}	–	2	5	mA	V_{DD} = +12V V_{RF} = +5V V_{SX} = −5V V_{CS} = 12V
Supply Current (Unselected) T_{AMB} = 70°C	I_{DDU}	–	4.5	15	mA	
Substrate Current	I_{SX}	–	−2.2	−3	mA	
Reference Supply Current	I_{RF}	–	50	100	μA	
Standby Current at Reduced Voltages T_{AMB} = 25°C	I_{DDS}	–	0.8	2	mA	V_{CS} = 4V to 15V V_{DD} = 4V V_{SX} = −5V ±10% V_{RF} = 0V
Standby Current at Reduced Voltages T_{AMB} = 70°C	I_{DDS}	–	1.8	6	mA	

AC ELECTRICAL CHARACTERISTICS (Full Operating Voltage and Temperature Range Unless Otherwise Noted)

Characteristics	Symbol	Min	Typ	Max	Unit	Figure
Chip Select Read Pulse Width	T_{CSR}	215ns	–	1ms	–	1
Chip Select Write Pulse Width	T_{CSW}	215ns	–	1ms	–	2
Chip Select Rise and Fall Time	T_{CR}, T_{CF}	–	10	50	ns	1&2
Set Up Time	T_P	0	–	–	ns	1&2
Access Time	T_A	–	–	215	ns	1
Cycle Time, T_{CR} = T_{CF} =10ns (Read or Write)	T_C	400	–	–	ns	1&2
Data Hold Time	T_H	100	–	–	ns	1&2
Output Recovery Time	T_{DR}	10	15	–	ns	1
Read Recovery Time	T_{CRR}	150	–	–	ns	1
Write Recovery Time	T_{CWR}	150	–	–	ns	2

CAPACITANCE (Over Full Temperature Range and Worst Case Voltage Conditions)

Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Input Capacitance (Except Chip Select)	C_{IN}	–	6	–	pF	V_{IN} = 2.4V
Input Capacitance Chip Select	C_{CS}	–	20	–	pF	V_{CS} = 12V or 0V
Output Capacitance	C_O	–	8	–	pF	V_O = 2.7V V_{CS} = 12V

DEVICE OPERATION

Basic Operation

The 4096 static bits of memory are organized in an array of 64 rows by 64 columns. The memory cells are loaded or interrogated by simultaneously decoding the X address A_0 through A_5 for the rows (see Block Diagram) and the Y address A_6 through A_{11} for the columns. Each column contains a presense amplifier, the outputs of which are "OR-ed" and connected to the output TTL buffer. Each bit or memory cell is a standard flip flop consisting of R_1, R_2, Q2D, and Q4D with two access devices Q1D and Q3D (See Figure 4). The load resistors R_1 and R_2 are 60 megohms typical and connect to the V_{DD} supply. Q1D and Q3D are used to connect the cell to the sense lines whenever the X access line is high. In the read mode the cell pulls one of the sense lines low from its normally high state. The selected presense circuit detects the differential voltage on the sense lines and amplifies it. In the write mode one sense line is forced low by the presense circuit and the selected cell assumes the state of the sense lines.

Chip Select

The Chip Select controls the operation of the memory. When the Chip Select input is high the input address buffers, decoders, sensing circuits and output stages are held in the "off" state and power is supplied only to the memory elements. When the Chip Select input is pulled low, the memory is enabled. The Chip Select negative going edge clocks the TTL logic level addresses $\overline{R}/W$, and data input into "D" type flip flops, and enables the output stage.

Data Output

While Chip Select is high, the output is high impedance to allow "wire-or" connections. When Chip Select goes low, the output data will be presented within the specified access time, and will remain until Chip Select goes high again. The output data signal is specified to drive any TTL series with good noise immunity at a fan-out of 1. Output data is inverted with respect to the input data.

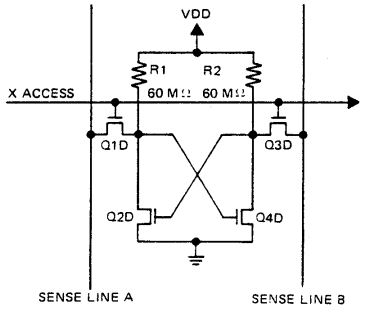


Figure 4. MEMORY CELL

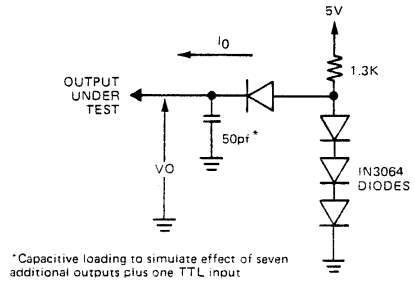


Figure 5. OUTPUT TEST LOAD

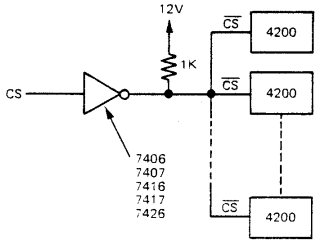


Figure 6. TYPICAL CHIP SELECT DRIVER

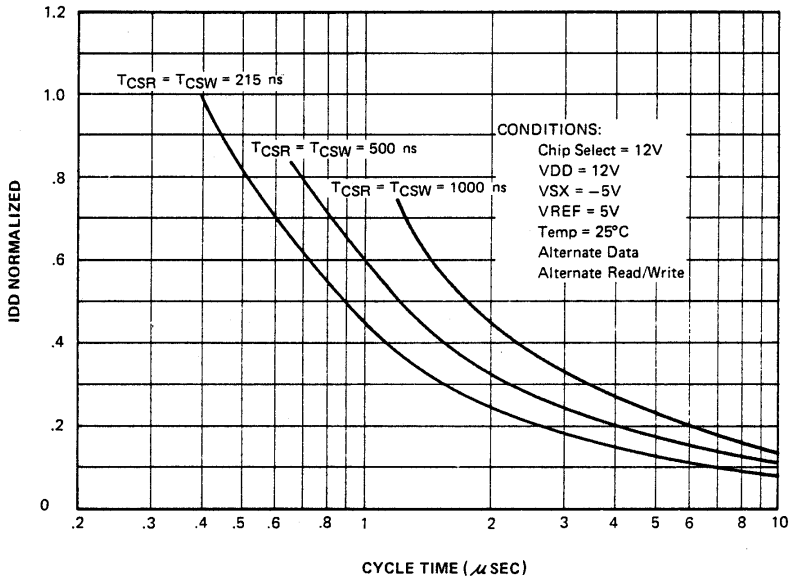


Figure 3. OPERATING I_{DD} AS A FUNCTION OF CYCLE TIME

BLOCK DIAGRAM